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EXAMINER	
GARCIA OTERO, EDUARDO	

ART UNIT	PAPER NUMBER
2123	18

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/418,663	Applicant(s) HAKEWILL ET AL.	
	Examiner Eduardo Garcia-Otero	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-22,40-42,47,48 and 60-78* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-22,40-42,47,48 and 60-78* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a)☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4)☐ Interview Summary (PTO-413) Paper No(s). _____.
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: .

DETAILED ACTION: Non-Final (first action after RCE)

Introduction

1. Title is: METHOD AND APPARATUS FOR MANAGING THE CONFIGURATION AND FUNCTIONALITY OF A SEMICONDUCTOR DESIGN.
2. Applicants are: HAKEWILL et al.
3. This action is in response to Applicant's request for continued examination, received 10/16/03.
4. Applicant cancelled claims 23-27, and amended claim 18 by inserting "relating to a basecase processor configuration".
5. The pending claims are 12-22, 40-42, 47-48, and 60-78.
6. Applicant claims priority to provisional application 60/104,271 filed Oct. 14, 1998.

Index

7. **Dangelo'678** refers to Dangelo et al. US Patent 6,324,678 B1.
8. **Dupenloup'123** refers to Dupenloup et al. US Patent 6,378,123 B1.
9. **Wirthlin'434** refers to Wirthlin et al. US Patent 6,173,434.
10. **Dangelo'958** refers to Dangelo et al. US Patent 5,801,958.
11. **Rostoker'399** refers to Rostoker et al. US Patent 5,867,399.
12. **Cambell** refers to Cambell et al., "A tutorial for make", Proceedings of the 1985 ACM annual conference on the range of computing: mid-80's perspective, 1985, Denver, Colorado, United States. Pages 374-380. ISBN 0-89791-170-9.
13. **Gupte'474** refers to Gupte et al. US Patent 5,903,475.
14. **Heile'369** refers to Heile et al. US Patent 6,321, 369.
15. **Turino'892** refers to Turino et al. US Patent 5,994,892.
16. **Smith** refers to "HDL Chip Design" by Douglas J. Smith, Ninth printing July 2001, minor updates. First Printing June 1996. Doone Publications. ISBN 0-9651934-3-8. pages 1-25.

APPLICANT REMARKS

17. SPECIFICATION OBJECTION WITHDRAWN. Remarks page 12. The Applicant has amended the specification at page 13 line 14 to now read "wizard", and persuasively asserts that "wizard" is a generic term for certain user-interactive routines, such as installation "wizards". Thus, the prior objection is withdrawn.

18. CLAIM 12. Remarks, page 13-16. Applicant asserts that that claim 12 (previously presented) "operates at a high level of abstraction", and that "Dangelo'678 specifically teaches away from high levels of abstraction". As supporting evidence, Applicant cites:
19. Dangelo'678 Abstract "*A method for generating structural descriptions of complex digital devices from high level descriptions and specifications is disclosed*", and
20. Dangelo'678 Column 2 line 46-49 "*A methodology for deriving a lower-level, physically implementable description, such as a RTL description of the higher level (e.g., VHDL) description, via an intermediate rule-based tool such as Prolog, is discussed herein*".
21. Additionally, Applicant asserts "Dangelo'678 is aimed only at lower levels of design abstraction", and asserts "the activities performed within Dangelo are all below the HDL/RTL level".
22. There appears to be some confusion with terminology regarding abstractions and languages, which the Examiner will attempt to clarify below.
23. LEVELS OF ABSTRACTION. There are 6 levels of abstraction per Smith FIG 1.2: System concept, Algorithm, Architecture, RTL (register transfer level), Gate, and Transistor. Note that Smith FIG 1.3 and FIG 1.5 define the levels of abstraction slightly differently: System, Algorithm, RTL, Logic, and Gate.
24. LANGUAGES. HDL refers to Hardware Description Languages which are often used for integrated circuit design. The "two industry standard hardware description languages" are "VHDL and Verilog" according to Smith page 3.
25. See the historical discussion at page 8. VHDL stands for "VHSIC Hardware Description Language", which in turn stands for "Very high speed integrated circuit Hardware Description Language". VHDL was revised in 1993 to IEEE 1076'93. Similarly, Verilog was adopted by IEEE as IEEE standard 1364 in 1995.
26. Note that Smith page 10 states "The modeling constructs of VHDL and Verilog cover a slightly different spectrum across the levels of behavior abstraction; see Figure 1.5." Said FIG 1.5 shows that Verilog models 4 levels of abstraction (Algorithm, RTL, Logic, and Gate), and that VHDL models 4 different levels of abstraction (System, Algorithm, RTL, and Logic). Thus, apparently Verilog cannot model the System level of abstraction, and VHDL cannot model the Gate level of abstraction. However, note that each HDL can model 4 levels

of abstraction. Further, note that Smith page 7 FIG 1.3 and FIG 1.4 show an iterative and top-down design process, starting at high level and progressing to low level. Also see Dangelo FIG 16a which shows progression through 4 levels of abstraction: "HIGHEST LEVEL", "MEDIUM-HIGH", "MEDIUM-LOW", "LOWEST LEVEL".

27. HIGHER LEVEL REPRESENTATION. Remarks page 13-14. Applicant asserts "the Dangelo'678 invention is meant to take a higher level representation (e.g., RTL or VHDL) of a design, and render a lower level description therefrom." Underline added. Applicant's statement is inconsistent. First, note that VHDL (Very high speed integrated circuit Hardware Description Language) is a hardware description language capable of 4 levels of abstraction per Smith FIG 1.5. Second, RTL appears to be relatively a lower level or middle level of abstraction (see Dangelo FIG 16a "MEDIUM-HIGH... MEDIUM-LOW"), and certainly lower level than System or Algorithm levels (in view of Smith FIG 1.3 and 1.5). Thus, Applicant's term "e.g., RTL or VHDL" is problematic, and appears to confuse two different concepts. RTL is a **middle or low level of abstraction**. VHDL is considered a **"high level" language** that it is capable of describing 4 levels of abstraction. "Levels" of computer languages has a very different meaning than "levels" of abstraction. In computer languages, the adjective "high level" indicates that the language must be translated or compiled into a machine language before execution.
28. Thus, the Examiner finds Applicant's interpretation of Dangelo'678 to be unpersuasive, and also indicative of problems with the terminology. These problems may be partly due to inconsistent terminology within the industry, as exemplified by Smith's inconsistent terminology for the levels of abstraction. Additionally, and somewhat confusingly, VHDL and Verilog are often described as "high level" languages (see Dangelo'678 column 3 line 51). However, note that each of said HDL languages can operate at 4 levels of abstraction. **Perhaps the best solution is to avoid describing VHDL and Verilog as "high-level language" in the context of simultaneously discussing levels of abstraction.**
29. INTERPRETATION. In the Examiner's opinion, Dangelo'678 Column 2 line 46-49 "*A methodology for deriving a lower-level, physically implementable description, such as a RTL description of the higher level (e.g., VHDL) description, via an intermediate rule-based tool such as Prolog, is discussed herein*" should be interpreted as **"a methodology for taking a**

high abstraction level HDL description (such as System level or Algorithm level, written in an industry standard language such as Verilog or VHDL which have capability of describing high abstraction levels) and deriving a lower abstraction level RTL description by using a rule-based tool such as Prolog". The Examiner's interpretation is also consistent with Dangelo'678 Abstract first sentence "methodology for generating structural descriptions of complex digital devices from high-level descriptions", and consistent with Dangelo'678 column 4 line 27 "An important feature of the present invention is that, as with all top-down design approaches, the foregoing is a process of architectural refinement in which design realization moves down through levels of abstraction. The characteristics of VHDL and the disclosed methodology enable this process to occur without losing the intent and meaning present at higher levels. This is the key to automating the process". The Examiner's interpretation is also consistent with the top two functional blocks of Smith FIG 1.4 "Typical ASIC design flow using simulation and RTL level synthesis". The first said functional block states "High level HDL specification", and the second functional block states "RTL code design-for-test". In summary, it appears to be standard procedure in integrated chip design to begin with high abstraction level descriptions and iteratively progress to lower abstraction levels. Also see Smith FIG 1.3.

30. **Thus, Dangelo'678 clearly teaches designing from high level to low level of abstraction.**

31. HIGH LEVEL. Applicant asserts that the claim 12 act of creating "editing a first file specific to said design; defining the location of at least one library file; generating a script using said fist file, said library file, and user information; and running said script to create said customized description language model" are performed at a high level of abstraction, and asserts that Dangelo'678 only discloses these limitations as low levels of abstraction. The Examiner finds these assertions unpersuasive. For example, **"editing a first file specific to said design"** is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL... next... starting with the VHDL behavioral description", and at Dangelo'678 FIG 2 showing iterative modifications to the design. Note that Dangelo'678 column 3 line 49 to column 4 line 20 discusses the progression of the design from "behavioral simulation" to "partitioning... architectural blocks" to "logic synthesis" to "physical simulation... the gate-level". Thus, the

design begins at a high level of abstraction, and iteratively progresses to lower levels of abstraction, and eventually down to the gate level. This same "top-down" process is similar to Smith FIG 1.3 and 1.4, and Smith page 6 "A top-down design methodology takes the HDL model of hardware, written at a high level of behavioral abstraction (system or algorithmic), down through intermediate levels, to a low (gate or transistor) level; Figure 1.2."

32. DUPENLOUP'123. Remarks page 14. Applicant asserts "Applicant's invention resides at the higher levels of abstraction". However, the claim 12 "high level of abstraction" limitation only applies to the "editing, defining, generating a script, running said script" portions of claim 12, and not to the limitations disclosed by Dupenloup'123. For example, the claim 12 limitation "**fabricating said integrated circuit using said at least one mask**" is disclosed by Dupenloup'123 at Column 79 line 66 "wafer corresponding to the pattern on the mask". Mask fabrication is not performed at high levels of abstraction.
33. WIRTHLIN'434. Remarks page 14. Remarks page 14. Applicant asserts "Applicant's invention resides at the higher levels of abstraction". However, the claim 12 "high level of abstraction" limitation only applies to the "editing... defining... generating a script... running said script..." portions of claim 1. The dependent claim 13 limitation "**custom instruction sets**" is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".
34. SECONDARY CONSIDERATIONS. Remarks page 15. Applicant asserts "secondary considerations have long been considered probative by the U.S. Supreme Court in determining patentability". Secondary considerations are "probative" in the sense of tending to prove, but not necessarily in the sense of actually proving an issue. This is a subtle distinction. See Black's Law Dictionary, "probative evidence", and "probative facts", and "probative value". Rather, *Graham v. John Deere* more clearly states "secondary considerations... may have relevancy". See MPEP 2141, MPEP 716.01(a), and *Minnesota Mining and Manufacturing Co. v. Johnson & Johnson Orthopedics, Inc.*, 24 USPQ 2d 1321 (Fed. Cir. 1992).
35. Applicant asserts that the instant claimed invention is commercially embodied in its Architect™ product, as an automated and user interactive high-level design tool. Applicant

further asserts that LSI Logic (assignee of Dangelo'678 and Dupneloup'123) has licensed its products. These assertions raise several issues.

36. ARCHITECT™, NEW ISSUES. First. The Examiner requests a copy of the earliest User's Manual for the Architect™ product which is the embodiment of the instant claimed invention.

37. Second. In accordance with 35 USC 102(b) and with 37 CFR 1.56, the **Examiner requests** all relevant information regarding whether **"the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States".**

38. Third. The Applicant never clearly states any details regarding the "great commercial success" of the commercial embodiment of the instant application. For example, the Applicant discusses "continued commercial success in licensing its products to a multitude of entities", but does not explicitly discuss the commercial success of the specific product which embodies the instant application. Further, no evidence is presented supporting the assertion of "satisfied a long-felt need".

39. The Examiner clearly contrasts Applicant's weak evidence of commercial success against the strong evidence and "colorful picture" presented in *Minnesota Mining* (see Page 1335). In *Minnesota Mining,* the "tremendous commercial success" included "revenues increased from $4.7 million in 1980 to over $15 million in 1981" (see page 1334). Further, the license was issued to a competitor who had failed to make a similar product with different material (see pages 1333-1335). Thus, the Examiner has carefully considered the present objective evidence, and hereby assigns this evidence very little weight.

40. Fourth, regarding automation of design, *In re Venner*, 262 F.2d 91, 95, 120 USPQ 192, 194 (CCPA 1958) states "it is well settled that it is not "invention" to broadly provide a mechanical or automatic means to replace manual activity which has accomplished the same result." Additionally, MPEP 2144.04(III) states "broadly providing an automatic or mechanical means to replace a manual activity which accomplished the same result is not sufficient to distinguish over the prior art." Thus, mere broad automation is not sufficient.
41. Fifth, if the Applicant provides additional evidence regarding commercial success or long-felt need of this instant invention as presently claimed, then the Examiner will consider the additional evidence carefully. A specific mapping of claim limitations to the commercial product would be very useful.
42. CLAIMS 18 AND 78. BASECASE PROCESSOR CONFIGURATION. Remarks page 16. Claim 18 has been amended to insert the term "relating to a basecase processor configuration". Said term is also present in claim 78. Applicant persuasively asserts that Wirthlin'434 is directed at PLAs (programmable logic arrays), and does not disclose "basecase processor configuration", and thus the prior rejection of claim 78 is not valid.
43. Therefore, the rejections of claim 18 (presently amended) and claim 78 (previously presented) are amended below to clearly address "basecase processor configuration".

Claim Interpretation

44. In claim 12, the term "creating is performed at a **high level of abstraction**" is interpreted as System level of abstraction or Algorithm level of abstraction, and not interpreted as "high level language".
45. In general (default interpretation), the Examiner interprets "high level" as referring to high levels of abstraction, specifically system level abstraction or algorithm level abstraction. The exception to this general rule occurs when "high level" is used to describe a language, then the Examiner interprets this term as describing integrated circuit industry standard languages (such as VHDL and Verilog) capable of describing four levels of abstraction. Note that "high level abstraction" and "high level language" are distinct concepts, because said "high level languages" can each actually describe 4 levels of abstraction, ranging from high to low levels of abstraction. In computer languages, the adjective "high level" indicates that the

language must be translated or compiled into a machine language before execution, as discussed above in Remarks section. These are distinct concepts.

Claim Rejections - 35 USC § 103

46. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

47. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

> Determining the scope and contents of the prior art.
>
> Ascertaining the differences between the prior art and the claims at issue.
>
> Resolving the level of ordinary skill in the pertinent art.
>
> Considering objective evidence present in the application indicating obviousness or nonobviousness.

48. Claims 12-22, 40-42, 47-48, and 60-78 are rejected under 35 U.S.C. 103(a) as being unpatentable.

49. Claim 12 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

50. Claim 12 is in independent claim with 8 limitations.

51. A-**editing a first file specific to said design** is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL", and at FIG 2 showing iterative modifications to the design.

52. B-**defining the location of at least one library file** is disclosed by Dangelo'678 at FIG 8 element 818 "CDE/SY LIBRARIES".

53. C-**generating a script using said first file, said library file, and user input information** is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

54. D-**running said script to create said customized description language model** is disclosed by Dangelo at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

55. E-**generating a netlist which is descriptive of the circuitry of said integrated circuit** is disclosed by Dangelo'678 at Column 49 line 55 "creating a netlist".

56. F-**compiling said netlist and said hardware description model to produce a compiled integrated circuit design** is disclosed by Dangelo'678 at Column 49 line 56 "compiling and simulating the netlist".

57. G-**fabricating at least one mask representing said compiled integrated circuit design** is disclosed by Dangelo'678 at Column 41 line 59 "mask level".

58. I-**wherein said act of creating is performed at a high level of abstraction is disclosed** is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL". Note that Applicant's term "creating" refers to limitations A-D, which are inherently performed at a high level of abstraction. This limitation may be redundant.

59. Dangelo'678 does not expressly disclose "fabricating said integrated circuit using said at least one mask".

60. H-**fabricating said integrated circuit using said at least one mask** is disclosed by Dupenloup'123 at Column 79 line 66 "wafer corresponding to the pattern on the mask".

61. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Dupenlup'123 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this fabricate the design that Dangelo'678 produced, because optical masks and photoresist on silicon wafers is the standard way to produce integrated circuits. Although Dangelo'678 does not explicitly discuss fabrication, it is implicit that Dangelo's IC design will be fabricated according to standard methods (after simulation testing and so forth).

62. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123 and Wirthlin'434.

63. Claim 13 depends from Claim 12 (amended), with four additional limitations.

64. **(ii)cache configurations** is disclosed by Dangelo'678 at Column 9 line 25 "functional specifications of subsystem elements", and Dangelo'678 at Column 13 line 37 "memory, mega-cells, mega-functions" (and also is disclosed by Dupenloup'123 at Column 78 line 33-44 "An exemplary integrated circuit...one or more randam access memories (RAM) 830").
65. **(iii)memory interface configurations** is disclosed by Dangelo'678 at Column 9 line 27 "interface requirements".
66. **(iv)system architecture configurations** is disclosed Dangelo'678 at Column 43 line 55 "architecture synthesis system".
67. Dangelo'678 does not expressly disclose custom instruction sets.
68. **(i)custom instruction sets** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".
69. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Dupenloup'123 and Wirthlin'434 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to allow "additional cycles for instructions that need significantly more time than traditional low-level instructions" according to Wirthlin'434 at Column 10 line 36, and to fabricate the design that Dangelo'678 produced.
70. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.
71. Claim 14 depends from Claim 12 (amended), one additional limitations.
72. **generating a list of logic devices and their interconnections** is disclosed by Dangelo'678 at Column 49 line 55 "creating a netlist".
73. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.
74. Claim 15 depends from Claim 12 (amended), with one additional limitation.
75. Dangelo does not expressly disclose lithographic process.
76. **defining physical features on a semi-conductive substrate via a lithographic process** is disclosed by Dupenloup'123 at Column 79 line 58 to Column 80 line 1 "Photolithography...semiconductor material".

77. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Dupenloup'123 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to fabricate the design that Dangelo'678 produced.
78. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.
79. Claim 16 depends from Claim 12 (amended), with one additional limitation.
80. **synthesizing said design based on said description language model** is disclosed by Dangelo'678 at Column 4 line 6 "logic synthesis".
81. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123 and Dangelo'958.
82. Claim 17 depends from Claim 13, with one additional limitation.
83. **editing is performed interactively with the user using a display** is disclosed by Dangelo'958 at Column 10 line 45 "user input occurs by pointing with the pointing device and selecting connection nodes, nets or devices and issuing commands which affect the selected object's numerical parameters". Note that Dangelo'958 "point and select" inherently discloses: a display, a pointer, and related graphical user interface software. Dangelo's "point and select" precisely discloses interactive editing, where the user interacts with a display using a pointer and related software.
84. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Dupenloup'123 and Dangelo'958 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to fabricate the design that Dangelo'678 produced, and to facilitate the user interaction with the editing program. Graphical user interfaces including "point and click" menus are universally recognized as efficient ways to interact with computers. For example, graphical user interfaces including a pointing mouse and clicking menus have been standard even on cheap personal computers for approximately 8 years.
85. Claim 18 (presently amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.
86. Claim 18 (presently amended) is an independent "apparatus" claim with 7 limitations.

87. D-**a computer program resident at least in part on said storage device, said computer program adapted to receive said input relating to a constrained set of design variables relating to a basecase processor configuration from said user and perform the following acts on said input: editing a first file specific to said integrated circuit design** is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL", and column 9 line 29 "Design Description. This is the functional description of the design and all its subsystem elements. The description is, ideally, given in a high level description language, such as VHDL. Depending on the nature of the design, the description can be entirely at the behavioral level, or it may be intertwined with an RTL description", and column 9 line 1 "The mega-cell and mega-function block 116 is chosen from pre-designed building block libraries, which are already designed for optimal performance" and FIG 12 "PREDESIGNED BLOCKS", and FIG 8 element 818 "LIBRARIES", and FIG 18 element 1810 "COMPONENT DATABASE".
88. E-[a computer program resident...] **defining the location of at least one library file** is disclosed by Dangelo'678 at FIG 8 element 818 "CDE/SY LIBRARIES".
89. F-[a computer program resident...] **generating a script using said first file, said library file, and user input information** is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".
90. G-[a computer program resident...] **running said script to create said description language model of said integrated circuit design** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".
91. Dangelo'678 does not expressly disclose processor, storage device, and input device.
92. A-**a processor capable of running a computer program** is disclosed by Dupenloup'123 at FIG 46 element 952 MICROPROCESSOR.
93. B-**a storage device being capable of storing at least a portion of a computer program** is disclosed by Dupenloup'123 at FIG 46 element 958 MASS STORAGE.
94. C-**an input device, operatively coupled to said processor, capable of receiving input from a user and transmitting said input to said processor** is disclosed by Dupenloup'123 at FIG 46 element 964 INPUT DEVICE.

95. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to Dupenloup'123 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to make the Dangelo'678 design process faster, cheaper, and with less errors.

96. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

97. Claim 19 depends from Claim 18 (amended), with one additional limitation.

98. said description language model is a hardware description language (HDL) is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL".

99. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

100. Claim 20 depends from Claim 18 (amended), with two additional limitations.

101. **generating a second file based on said description language model for use with a simulation** is disclosed by Dangelo'678 at Column 1 line 53 "information necessary for layout, verification and simulation into a schematic object file or files".

102. simulating said design using said second file is disclosed by Dangelo'678 at Column 1 line 61 "generates a set of simulation results".

103. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

104. Claim 21 depends from Claim 20, with one additional limitation.

105. running synthesis scripts based on said description language model in order to synthesize said integrated circuit design is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

106. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

107. Claim 22 depends from Claim 18 (amended), with two additional limitations.

108. Dangelo'678 does not expressly disclose digital microprocessor and magnetic media storage device.

109. **said processor comprises a digital microprocessor** is disclosed by Dupenloup'123 at FIG 46 element 952 MICROPROCESSOR.

110. **said storage device comprises magnetic media** is disclosed by Dupenloup'123 at FIG 46 element 958 MASS STORAGE.

111. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to Dupenloup'123 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to make the Dangelo'678 design process faster, cheaper, and with less errors.

112. Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123 and Wirthlin'434.

113. Claim 40 is an independent "system" claim (or "machine" per 35 USC 101), with 8 limitations.

114. **4-(ii) a plurality of cache configurations** is disclosed by Dangelo'678 at Column 9 line 25 "functional specifications of subsystem elements", and Dangelo'678 at Column 13 line 37 "memory, mega-cells, mega-functions" (and also is disclosed by Dupenloup'123 at Column 78 line 33-44 "An exemplary integrated circuit...one or more random access memories (RAM) 830").

115. **5-(iii) a plurality of memory interface configurations** is disclosed by Dangelo'678 at Column 9 line 27 "interface requirements".

116. Dangelo does not expressly disclose "custom instruction".

117. **6-(iv) a plurality of system architecture configurations** is disclosed Dangelo'678 at Column 43 line 55 "architecture synthesis system".

118. 7-a first algorithm capable of generating a script based on selections made by a user from said at least first user selectable element is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

119. **8-a second algorithm capable of running said script to generate a description language model of an integrated circuit design** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

120. Dangelo'678 does not expressly disclose limitations 1-3.

121. **1-a processor** is disclosed by Dupenloup'123 at FIG 46 element 952 MICROPROCESSOR

122. **2-a storage device in data communication with said processor** is disclosed by Dupenloup'123 at FIG 46 element 956 RAM.

123. **3-(i) a plurality of custom instructions** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

124. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Dupenloup'123 and Wirthlin'434 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to implement the procedure of Dagngelo'678 using the processor of Dupenloup'123, and to allow "additional cycles for instructions that need significantly more time than traditional low-level instructions" according to Wirthlin'434 at Column 10 line 36.

125. Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123 and Wirthlin'434 and Gupte.

126. Claim 41 depends from Claim 40, with one additional limitation.

127. Dangelo'678 does not expressly disclose the additional limitation.

128. **plurality of process technology options** is disclosed by Gupte at Column 4 line 60 "process technology".

129. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Dupenloup'123 and Wirthlin'434 and Gupte to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to implement the procedure of Dagngelo'678 using the processor of Dupenloup'123, and to allow "additional cycles for instructions that need significantly more time than traditional low-level instructions" according to Wirthlin'434 at Column 10 line 36, and to do this to save time and money by using the same circuit design methods for different process technologies.

130. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123 and Wirthlin'434 and official notice (and mere automation).

131. Claim 42 depends from Claim 40, with one additional limitation.

132. Dangelo'678 does not expressly disclose the additional limitation.

133. **pre-configured data file** is disclosed by official notice that it is well known in the art to store the detailed parameters of user selected elements in pre-configured data files.

134. Also, using pre-configured data files is **merely automating** the manual entry of said data. In re Venner, 262 F.2d 91, 95, 120 USPQ 192, 194 (CCPA 1958) states "it is well settled that it is not "invention" to broadly provide a mechanical or automatic means to replace manual activity which has accomplished the same result." Additionally, MPEP 2144.04(III) states "broadly providing an automatic or mechanical means to replace a manual activity which accomplished the same result is not sufficient to distinguish over the prior art."

135. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Dupenloup'123 and Wirthlin'434 and official notice of data files to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to implement the procedure of Dagngelo'678 using the processor of Dupenloup'123, and to allow "additional cycles for instructions that need significantly more time than traditional low-level instructions" according to Wirthlin'434 at Column 10 line 36, and to allow the user to quickly and accurately input large amounts of data in the form of pre-configured data files.

136. Claim 47 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Gupte and Wirthlin'434.

137. Claim 47 (amended) is an independent "method" claim with 9 limitations.

138. **3-(ii) cache configuration** is disclosed by Dangelo'678 at Column 9 line 25 "functional specifications of subsystem elements", and Dangelo'678 at Column 13 line 37 "memory, mega-cells, mega-functions" (and also is disclosed by Dupenloup'123 at Column 78 line 33-44 "An exemplary integrated circuit...one or more random access memories (RAM) 830").

139. **4-(iii) memory interface configuration** is disclosed by Dangelo'678 at Column 9 line 27 "interface requirements".

140. **5-(iv) system architecture configuration** is disclosed Dangelo'678 at Column 43 line 55 "architecture synthesis system".

141. 6-defining the location of at least one library file is disclosed by Dangelo'678 at FIG 8 element 818 "CDE/SY LIBRARIES".

142. **7-generating a script using said first file and said library** is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

143. **8-running said script to create a customized hardware description language model of the design** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

144. **9-running a synthesis algorithm to synthesize a file descriptive of said design** is disclosed by Dangelo'678 at Column 4 line 6 "logic synthesis".

145. Dangelo'678 does not expressly disclose 2 of the limitations.

146. **1-selecting a process technology** is disclosed by Gupte at Column 4 line 60 "process technology".

147. **2-(i) processor instructions** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

148. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Gupte and Wirthlin'434 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to use Gupte to save time and money by using the same design program for various technologies, and to use Wirthlin'434 to save time by customizing the clock cycles to match the level of complexity of the instructions.

149. Claim 48 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123 and Wirthlin'434.

150. Claim 48 (amended) is an independent "means for" claim with substantially the same limitations as Claim 40, thus is rejected for the same reasons.

151. Claim 60 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

152. Claim 60 (amended) is an independent method claim with 2 limitations.

153. **generating, at a high level of abstraction, a description of a hardware implementation of said configurable processor** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

154. Dangelo'678 does not expressly disclose one limitation:

155. **at least one user-defined instruction** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

156. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wirthlin'434 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to customize the timing to allow high-level instructions.

157. Claim 61 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

158. Claim 61 depends from Claim 60 (amended), with one additional limitation.

159. Dangelo'678 does not expressly disclose the additional limitation:

160. **generating a description including control logic necessary for the execution of said at least one user-defined instruction** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

161. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wirthlin'434 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to customize the timing to allow high-level instructions.

162. Claim 62 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

163. Claim 62 depends from Claim 61, with one additional limitation.

164. **instruction execution pipeline having a plurality of stages, said control logic including portions associated with said stages** is disclosed by Dangelo'678 at Column 27 line 22 "specific control elements are assigned to the control logic in the RT level description of the system".

165. Claim 63 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434 and Turino'892.

166. Claim 63 depends from Claim 60, with 3 additional limitations.

167. **(i)-registers** is disclosed by Dangelo'678 at Column 7 line 29 "registers".

168. **(iii)-scratchpad RAM** is disclosed by Dangelo'678 at Column 11 line 60 "RAM".

169. Dangelo does not disclose one limitation:

170. **(ii)-condition code choices** is disclosed by Turino'892 at Column 34 line 10 "Condition Code Register (CCR) - - 8 bits".

171. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wirthlin'434 and Turino'892 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to customize the timing to allow high-level instructions, and to minimize the number of bits in the condition code register.

172. Claim 64 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434

173. Claim 64 depends from Claim 60, with 1 additional limitation.

174. **at least one library of multimedia extensions** is disclosed by Dangelo'678 at Column 9 line 2 "libraries".

175. Claim 65 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434

176. Claim 65 depends from Claim 60, with 1 additional limitation.

177. **simulating said configurable processor** is disclosed by Dangelo'678 at Column 4 line 15 "simulation".

178. Claim 66 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

179. Claim 66 depends from Claim 65, with 3 additional limitations.

180. **running at least one script to generate simulation data** is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

181. **running at least one simulation using at least said simulation data** is disclosed by Dangelo'678 at Column 4 line 15 "simulation".

182. **determining the adequacy of said configurable processor based at least in part on said act of running** is disclosed by Dangelo'678 at Column 4 line 18 "This provides a check that the circuit implementation behaves as intended, and that the timing goals are achieved.

183. Claim 67 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434

184. Claim 67 depends from Claim 60, with 1 additional limitation.

185. synthesizing said configurable processor using at least said description is disclosed by Dangelo'678 at Column 4 line 6 "synthesis".

186. Claim 68 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

187. Claim 68 depends from Claim 67, with 2 additional limitations.

188. **running at least one synthesis script to generate synthesis data** is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

189. evaluating the adequacy of said synthesis data based at least in part on at least one design criterion is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

190. Claim 69 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

191. Claim 69 depends from Claim 68, with 2 additional limitations.

192. at least one processor die size criterion is disclosed by Dangelo'678 at Column 41 line 46 "die size".

193. Dangelo'678 does not expressly disclose one limitation:

194. at least one specific processor performance criterion is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

195. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wirthlin'434 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to customize the timing to allow high-level instructions.

196. Claim 70 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

197. Claim 70 depends from Claim 68, with 3 additional limitations.

198. **revising at least one design element when said act of evaluating indicates that said synthesis data is not adequate** is disclosed by Dangelo'678 at Column 5 line 32 "design is resynthesized until a design is arrived at that meets timing constraints".

199. re-running said at least one synthesis script using said at least one revised design element to generate revised synthesis data is disclosed by Dangelo'678 at Column 5 line 32 "design is resynthesized until a design is arrived at that meets timing constraints".

200. and re-evaluating the adequacy of said revised synthesis data based at least in part on said at least one design criterion is disclosed by Dangelo'678 at Column 5 line 32 "design is resynthesized until a design is arrived at that meets timing constraints".

201. Claim 71 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

202. Claim 71 depends from Claim 70, with 2 additional limitations.

203. **at least one processor die size criterion** is disclosed by Dangelo'678 at Column 41 line 46 "die size".

204. **revising at least one library** is disclosed by Dangelo'678 at FIG 8 element 818 "CDE/SY LIBRARIES".

205. Claim 72 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

206. Claim 72 depends from Claim 71, with 2 additional limitations.

207. **at least one processor die size criterion** is disclosed by Dangelo'678 at Column 41 line 46 "die size".

208. **revising at least one control file** is disclosed by Dangelo'678 at Column 27 line 22 "control elements".

209. Claim 73 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

210. Claim 73 depends from Claim 70, with 2 additional limitations.

211. **processor clock speed** is disclosed by Dangelo'678 at Column 10 line 52 "length of clock cycle"

212. **at least one library** is disclosed by Dangelo'678 at FIG 8 element 818 "CDE/SY LIBRARIES".

213. Claim 74 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

214. Claim 74 depends from Claim 70, with 2 additional limitations.

215. **processor power consumption** is disclosed by Dangelo'678 Column 19 line 47 "allows the user to perform a "what if" analysis for choosing a preferred design in terms of size, speed, performance, technology, and power".

216. **at least one netlist (net load)** is disclosed by Dangelo'678 Column 49 line 56 "compiling and simulating the netlist".

217. Claim 75 (new) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Gupte.

218. Independent claim 75 (new) is a method claim with 8 limitations.

219. A-**providing an existing core configuration** is disclosed by Dangelo'678 at Column 5 line 32 "design is resynthesized until a design is arrived at that meets timing constraints". Also see Dangelo'678 FIG 2 which illustrates the iterative nature of integrated circuit design.

220. B-**editing a first file specific to the design, said editing comprising selecting a constrained set of input parameters associated with said configuration, said parameters comprising: (i)at least one custom instruction** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line", and at Column 14 line 21 "dc-shell script and constraints files", and at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL", and at FIG 2 showing iterative modifications to the design.

221. E-**providing at least one library file** is disclosed by Dangelo'678 at FIG 8 element 818 "CDE/SY LIBRARIES".

222. F-**generating a script using said first file, said library file, and user input information** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

223. G-**running said script to create a customized description language model** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

224. H-**synthesizing said design based on said description language model** is disclosed by Dangelo'678 Column 49 line 56 "compiling and simulating the netlist".

225. Dangelo does not expressly disclose the additional limitations.

226. C-**(ii)a cache configuration** is disclosed by Gupte at Column 6 line 18 "cache memory".

227. D-**(iii) a memory interface configuration** is disclosed by Gupte at Column 6 line 18 "cache memory".

228. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Gupte to modify Dangelo'678. One of ordinary skill in the art would have been motivated to select cache configurations and memory interface configurations in order to customize the process of Dangelo'678 to quickly and cheaply design alternate combinations of configurations and instructions, and to increase the overall circuit performance speed by inserting a cache memory as a buffer.

229. Claim 76 (new) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Gupte.

230. Independent claim 76 (new) is a method claim with 7 limitations.

231. E-**generating a script based on said at least one optional instruction, cache instruction, and memory interface** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

232. F-**running said script to generate a hardware description language model of said integrated circuit design** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

233. Dangelo does not expressly disclose the additional limitations.

234. A-**providing a user with a plurality of optional instructions, including the ability to generate a customized instruction** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

235. B-**selecting at least one of said plurality of optional instructions** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional

cycles for instructions that need significantly more time than traditional low-level instructions".

236. C-**selecting at least one cache configuration** is disclosed by Gupte at Column 6 line 18 "cache memory".

237. D-**defining at least one memory interface** is disclosed by Gupte at Column 6 line 18 "cache memory".

238. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wirthlin'434 and Gupte to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to customize the timing to allow high-level instructions, and to apply Dangelo'678 design methods to cache memories to speed processing.

239. Claim 77 (new) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Gupte and Wirthlin'434.

240. Independent claim 77 (new) is a method claim with 7 limitations.

241. E-**generating a script based on said at least one optional instruction, cache configuration, and memory interface** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

242. F-**running said script to generate a hardware description language model of said integrated circuit design** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

243. Dangelo'678 does not explicitly disclose the additional limitations.

244. A-**editing a first file specific to said integrated circuit design including selecting a plurality of input parameters associated with said design, said parameters comprising: (i) at least one custom instruction set** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

245. B-**(ii) a cache configuration** is disclosed by Gupte at Column 6 line 18 "cache memory".

246. C-**selecting at least one cache configuration** is disclosed by Gupte at Column 6 line 18 "cache memory".

247. D-**defining at least one memory interface** is disclosed by Gupte at Column 6 line 18 "cache memory".

248. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wirthlin'434 and Gupte to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to customize the timing to allow high-level instructions, and to apply Dangelo'678 design methods to cache memories to speed processing.

249. Claim 78 (new) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Gupte and Wirthlin'434.

250. Independent claim 78 (new) is a method claim with 7 limitations.

251. A-**providing the user with a basecase processor configuration having a base instruction set** is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL", and column 9 line 29 "Design Description. This is the functional description of the design and all its subsystem elements. The description is, ideally, given in a high level description language, such as VHDL. Depending on the nature of the design, the description can be entirely at the behavioral level, or it may be intertwined with an RTL description", and column 9 line 1 "The mega-cell and mega-function block 116 is chosen from pre-designed building block libraries, which are already designed for optimal performance" and FIG 12 "PREDESIGNED BLOCKS", and FIG 8 element 818 "LIBRARIES", and FIG 18 element 1810 "COMPONENT DATABASE".

252. E-**generating a script based on said at least one optional instruction, cache configuration, and memory interface** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

253. F-**running said script to generate a hardware descriptive language model of said processor design** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE

programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

254. Dangelo'678 does not explicitly disclose the additional limitations.

255. B-**providing a user with a plurality of optional instructions adaptable for use with said basecase core** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

256. C-**selecting at least one cache configuration** is disclosed by Gupte at Column 6 line 18 "cache memory".

257. G-**wherein said plurality of optional and cache configurations are constrained so as to ensure the functionality of said processor design irrespective of the user's selection** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

258. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wirthlin'434 and Gupte to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to customize the timing to allow high-level instructions, and to apply Dangelo'678 design methods to cache memories to speed processing.

Conclusion

259. The prior objection to the specification is withdrawn.

260. All pending claims are rejected under 35 USC 103.

261. The Examiner requests the following: (1) the **earliest User's Manual for the Architect™** product which is the embodiment of the instant claimed invention, including a mapping of claim limitations to the product features, (2) all relevant information regarding the **first publication, public use, or sale of said product.**

Communication

262. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 703-305-0857. The examiner can normally be reached on Tuesday through Friday from 9:00 AM to

8:00 PM. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone number for this group is 703-872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

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